**Amendments to the Claims:**

This listing of claims will replace all prior versions and listings of claims in the application:

**Listing of Claims:**

1-11 (cancelled).

12 (previously presented): A control circuit of memory address decoding for determining whether a given address is located in one of a plurality of sections in memory, each memory section having at least one memory unit and each memory unit being associated with a unique binary address, the control circuit comprising:

a pattern calculation module for building at least one bit-pattern for each section based on the associated addresses;

an access module for receiving the given address; and

a comparing module for calculating a bit-pattern for each section based on the associated addresses, and sending a plurality of comparison signals after comparing at least one of the comparative bits in the given address with each bit-pattern provided by the pattern calculation module respectively, wherein the comparing module comprises a plurality of comparing units, each comparing unit comprising a plurality of NAND gates and one single AND gate, each of the NAND gates having two inputs for respectively receiving one bit of the bit-patterns and another bit associated with the given address, the inputs of the NAND gate being connected to the outputs of the AND gate and thereby sending out the comparison signals.

13 (original): The control circuit of claim 12, further comprising a logic module responsible for receiving the comparison signals and sending a decoding result for determining the section in which the given address is located.

14 (original): The control circuit of claim 12 wherein the sections are a plurality of

memory modules.

15 (original): The control circuit of claim 12 wherein the sections are a plurality of rank memory arrays and an even number of rank memory arrays of the same size compose a memory module.

16 (original): The control circuit of claim 12 wherein at least one bit-pattern is built for each section in the pattern calculation module, the bit-patterns consisting of all common bits of the associated addresses in each section.

17 (original): The control circuit of claim 12 wherein at least one bit-pattern is built for each section in the pattern calculation module, the bit-patterns consisting of partial common bits of the associated addresses in each section.

18 (cancelled).

19 (currently amended): A memory address decoding method for determining an objective section of a given address in a memory, wherein the memory is formed by at least one section, which comprises at least one memory unit having a corresponding address, the method comprising:

obtaining at least one bit-pattern according to a common pattern of bits of the addresses;

comparing the given address with each bit-pattern to determine the objective section of the given address;

comparing the given address with at least one ending address to determine an objective group of the objective section, wherein the ending address is substantially equal to the first address or the last address of each section; and

storing the objective group in memory.

20 (previously presented): The method of claim 19, wherein bits of the given address are correspondingly compared to the bit-pattern.

21 (previously presented): The method of claim 19, wherein each section comprises at least one bit-pattern.

22-23 (cancelled).

24 (currently amended): The method of ~~claim 22~~ claim 19, wherein the given address is compared with bit-patterns of the objective group.

25 (previously presented): The method of claim 19, wherein the bit-pattern is obtained by all common bits of the address in each section.

26 (previously presented): The method of claim 19, wherein the bit-pattern is obtained by partial common bits of the address in each section.

27 (previously presented): The method of claim 19, wherein the given address is located in the objective section when bits of the given address completely match the bit-pattern of the objective section.

28 (previously presented): The method of claim 19, wherein each section is formed by at least one memory module.